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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/092,056	03/05/2002	Deepak Sabharwal	1263-0014US	7809

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EXAMINER
TAT, BINH C

ART UNIT	PAPER NUMBER
2825	

DATE MAILED: 08/21/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/092,056	SABHARWAL ET AL.	
	Examiner	Art Unit	
	Binh C. Tat	2825	

-- Th MAILING DATE of this communication appears on the cov r sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *05 March 2002* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-49* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-49* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *05 March 2002* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☒ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

1. This office action is in response to application 10/092056 filed on 03/05/02.

Claims 1-49 remain pending in the application.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

2. Claims 1-49 are rejected under 35 U.S.C. 102(e) as being anticipated by Lipovski (US Patent 6460166).

3. As to claims 1 (method), 22 (system) and 35 (machine-readable medium), Lipovski teaches a memory characterization method, comprising the steps generating a plurality of tiles forming a memory instance, said plurality of tiles including at least one of a sub-plurality of row decoder tiles, a sub plurality of input/output (I/O) block tiles, a sub plurality of bitcell array tiles and at least one control block tile (see fig 2 and fig 5 element 13 col 8 lines 35-53); providing input and output pins for each tile to with respect to a plurality of global signals spanning said memory instance in at least one of a horizontal and a vertical direction (see fig 2 and fig 5 and fig 6); obtaining a parametric dataset for each of said plurality of tiles (see col 9 lines 3-45); and creating a hierarchically-stitched parametric netlist for said memory instance by coupling said

parametric datasets using said .input and output pins of said plurality of tiles with respect to said global signals (see fig 2 and fig 5 and fig 6 col 9 lines 3-45).

4. As to claims 2 (method), and 49 (machine-readable medium), Lipovski teach wherein said tiles are generated based on a minimum area required to encompass an optimal number of memory strap points associated with at least a portion of said global signals (see fig 5-6 col 9 and background).

5. As to claims 3, 6 (method), and 36 (machine-readable medium), Lipovski teach wherein said memory instance comprises a post-layout schema, and further wherein said step of obtaining a parametric dataset for each of said plurality of tiles comprises extracting an RC netlist from a select portion of: said post-layout schema corresponding to a particular tile (see fig 7 col 10 lines 20-48).

6. As to claims 4, 5 (method), 23 (system) and 37 (machine-readable medium), Lipovski teach wherein said memory instance comprises a pre layout schema, and further wherein said step of obtaining a parametric dataset for each of said plurality of tiles comprises estimating RC parametric data corresponding to a particular tile based on its wire-delay model circuit (see fig 5-6 background/summary).

7. As to claims 7-10 Lipovski teach wherein wherein said plurality of tiles are generated from a memory instance comprising a read-only memory (ROM), (RAM), (DRAM), and (EPROM) circuit (see fig 5-6 background/summary).

8. As to claims 11 (method), 24 (system) and 38 (machine-readable medium), Lipovski teach wherein said plurality of tiles are generated from a memory instance comprising a flash memory circuit (see fig 5-6 background/summary).

9. As to claims 12 (method), 26 (system) and 40 (machine-readable medium), Lipovski teach wherein said plurality of tiles are generated from a memory instance comprising a compilable memory circuit (see fig 5-6 background/summary).

10. As to claims 13 (method), 25 (system) and 39 (machine-readable medium), Lipovski teach wherein said plurality of tiles are generated from a memory instance comprising an embedded memory circuit (see fig 5-6 background/summary).

11. As to claims 14 (method), 27(system) and 41 (machine-readable medium), Lipovski teach wherein said plurality of tiles are generated from a memory instance comprising a stand-alone memory circuit (see fig 5-6 background/summary).

12. As to claims 15 (method), 28 (system) and 42 (machine-readable medium), Lipovski teach wherein said global signals comprise a plurality of pre-decoder signals emanating from said at least one control block tile, said pre-decoder signals being operable to couple said sub-plurality of row decoder tiles in a head-to-tail fashion along said vertical direction (see fig 5-6 and col 9-10 background/summary).

13. As to claims 16 (method), 29 (system) and 43 (machine-readable medium), Lipovski teach wherein each row decoder tile is coupled to a corresponding portion of said plurality of wordline signals, said corresponding portion being operable to couple a select row of said sub-plurality of bitcell array tiles in a head-to-tail fashion along said horizontal direction (see fig 5-6 and col 9-10 background/summary).

14. As to claims 17 (method), 30 (system) and 44 (machine-readable medium), Lipovski teach wherein each row decoder tile is coupled to a corresponding portion of said plurality of wordline signals, said corresponding portion being operable to couple a select row of said

sub-plurality of bitcell array tiles in a head-to-tail fashion along said horizontal direction (see fig 5-6 and col 9-10 background/summary).

15. As to claims 18 (method), 31 (system) and 45 (machine-readable medium), Lipovski teach wherein said global signals comprise a plurality of control signals emanating from said at least one control block tile, said control signals being operable to couple said sub-plurality of I/O block tiles in a head-to-tail fashion along said horizontal direction (see fig 5-6 and col 9-10 background/summary).

16. As to claims 19 (method), 32 (system) and 46 (machine-readable medium), Lipovski teach wherein said global signals comprise a plurality of bitline signals emanating from said sub plurality of I/O block tiles (see fig 5-6).

17. As to claims 20 (method), 33 (system) and 47 (machine-readable medium), Lipovski teach wherein each I/O block tile is coupled to a corresponding portion of said plurality of bitline signals, said corresponding portion being operable to couple a select column of said sub-plurality of bitcell array tiles in a head-to-tail fashion along said vertical direction (see fig 5-6 and col 9-10 background/summary).

18. As to claims 21 (method), 34 (system) and 48 (machine-readable medium), Lipovski teach wherein said global signals comprise a plurality of power lines coupling said sub-plurality of I/O block tiles with said sub-plurality of bitcell array tiles in said vertical direction (see fig 5-6 and col 9-10 background/summary).

Conclusion

19. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Binh C. Tat whose telephone number is (703) 305-4855. The examiner can normally be reached on 7:30 - 4:00 (M-F).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mathew Smith can be reached on (703) 308-1323. The fax phone numbers for the organization where this application or proceeding is assigned are (703) 305-3431 for regular communications and (703) 305-3431 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 308-1782.

Binh Tat BT
Art Unit 2825
August 9, 2003

H. M. THOMPSON
MASTER'S LEVEL PATENT EXAMINER
TECHNOLOGY CENTER 2800